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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/495,150	01/31/2000	Gopal Hegde	30019.103US01	4464

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EXAMINER
DAY, HERNG DER

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/495,150	HEGDE ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-17 have been examined and claims 1-17 have been rejected.

Drawings

2. The drawings are objected to for the following reasons.

2-1. The Draftsperson has objected to the drawings; see the copy of Form PTO 948 for an explanation.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Bauer et al., "Hardware/Software Co-Simulation in a VHDL-based Test Bench Approach", Proceedings of the 34th Design Automation Conference, June 1997, pages 774-779.

4-1. Regarding claim 1, Bauer et al. disclose a method of developing an ASIC, comprising:

developing hardware and software concurrently (use the unit under test as a hardware model for the software test; software acts as a generator and analyzer for the unit under test, page 774, section 1, paragraph 4); and

co-simulating the hardware and software therebetween via a network while the hardware and software are being developed (TCP/IP, page 778, section 5.3, paragraphs 7-8).

4-2. Regarding claim 2, Bauer et al. further disclose that the hardware is developed on a workstation (same host as the VHDL tool, page 778, section 5.3, paragraph 4).

4-3. Regarding claim 3, Bauer et al. further disclose that the software is developed on a target board (test bench, page 778, section 6, paragraphs 2-3).

4-4. Regarding claim 4, Bauer et al. further disclose that the network is a TCP/IP protocol (TCP/IP, page 778, section 5.3, paragraphs 7-8).

4-5. Regarding claim 5, Bauer et al. further disclose that the hardware to be co-simulated is described by a high-level language model (VHDL simulator, page 778, section 5.3, paragraph 9).

4-6. Regarding claim 7, Bauer et al. further disclose receiving test inputs for the co-simulation from a test tool (Traffic Generator, page 779, Figure 3).

4-7. Regarding claim 8, Bauer et al. disclose a method of co-simulating hardware and software in ASIC development, comprising:

requesting an access to a hardware model from a hardware side to a software side via a network (software command, page 778, section 5.3, paragraph 6);

invoking a function call by a CPU server at a software side (calls the corresponding software routines, page 778, section 5.3, paragraph 6);

sending an access request from the hardware side to the CPU server at the software side via the network (via VHDL communication channels; to TCP/IP link, page 778, section 5.3, paragraph 6); and

routing the access request to the hardware model (to the micro processor model, page 778, section 5.3, paragraph 7).

4-8. Regarding claim 9, Bauer et al. further disclose that the function call is a READ function call (micro processor command; read operation, page 778, section 5.3, paragraph 7).

4-9. Regarding claim 10, Bauer et al. further disclose that the function call is a WRITE function call (micro processor command; write operation, page 778, section 5.3, paragraph 7).

4-10. Regarding claim 11, Bauer et al. further disclose requesting a hardware model interrupt, and a function call to handle the interrupt being invoked by the software via the network (If an interrupt occurs, an exception handling procedure is called, page 778, section 5.2, paragraph 4).

4-11. Regarding claim 12, Bauer et al. disclose an apparatus for hardware and software co-simulation in ASIC development comprising:

a hardware model to represent a hardware board circuit to be co-simulated/tested (VHDL simulator, page 778, section 5.3, paragraph 9), the hardware model being developed on a workstation (same host as the VHDL tool, page 778, section 5.3, paragraph 4);

a software to command and control accesses of the hardware model, the software being developed/debugged on a target board (test bench, page 778, section 6, paragraphs 2-3) concurrently with a design of the hardware model (use the unit under test as a hardware model for the software test; software acts as a generator and analyzer for the unit under test, page 774, section 1, paragraph 4); and

a network, coupled between the workstation and the target board, to communicate a command from the software to the hardware model and to route contents of the command between the workstation and the target board (TCP/IP, page 778, section 5.3, paragraphs 7-8).

4-12. Regarding claim 13, Bauer et al. further disclose that the hardware model comprises a CPU bus functional model which communicates the hardware model to a CPU server of the target board via the network (bus functional model, page 777, section 5.2, paragraph 1).

4-13. Regarding claim 14, Bauer et al. further disclose that the software is loaded on the CPU server (software server, page 778, section 5.3, paragraph 5).

4-14. Regarding claim 15, Bauer et al. further disclose that the network is a TCP/IP protocol (TCP/IP, page 778, section 5.3, paragraphs 7-8).

4-15. Regarding claim 17, Bauer et al. further disclose that the hardware model is capable of receiving test inputs for co-simulation from a test tool (Traffic Generator, page 779, Figure 3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et al., "Hardware/Software Co-Simulation in a VHDL-based Test Bench Approach", Proceedings of the 34th Design Automation Conference, June 1997, pages 774-779, in view of Rowson, "Hardware/Software Co-Simulation", Proceedings of the 31st ACM/IEEE Conference on Design Automation Conference, June 1994, pages 439-440.

6-1. Regarding claim 6, Bauer et al. disclose the hardware/software co-simulation in a project consists of four ASICs. However, Bauer et al. fail to expressly disclose receiving test inputs for the co-simulation from a real working environment.

Rowson discloses using hardware in place of a software model, i.e. using an actual part as the model, called by the simulator (page 440, column 1, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bauer et al. to receive test inputs through real hardware ports for the co-simulation from a real working environment to obtain the invention as specified in claim 6 because the inputs from a real working environment help the developer find the most common problems in an early stage of the developing process to save development cost. The purpose to develop ASIC products is to make them useful and marketable in a real working environment. If the developed ASIC products may not function correctly in a real working environment, co-simulation with inputs from a real working environment will help developers to find and correct problems in an early stage of the developing process to save development cost.

6-2. Regarding claim 16, Bauer et al. disclose the hardware/software co-simulation in a project consists of four ASICs where the hardware model is capable of receiving test inputs from the traffic generator. The purpose of traffic generator is to generate packets, which simulates the traffic compatible with a real working environment and has predetermined characteristics, to test the developed products. Bauer et al. fail to expressly disclose that the hardware model is capable of receiving test inputs for the co-simulation from a real working environment.

Rowson discloses using hardware in place of a software model, i.e. using an actual part as the model, called by the simulator (page 440, column 1, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bauer et al. to receive test inputs through real hardware ports for the co-simulation from a real working environment to obtain the invention as specified in claim 16 because through real hardware ports any hardware model being capable of receiving test inputs from the traffic generator will also be capable of receiving test inputs from a real working environment.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference to van Tetering et al., U.S. Patent 5,343,463 issued August 30, 1994, is cited as disclosing a method for measuring the performances characteristics of a communication path.

Reference to Denissen et al., U.S. Patent 5,450,400 issued September 12, 1995, is cited as disclosing a traffic generator.

Reference to Bunza, U.S. Patent 5,838,948 issued November 17, 1998, is cited as disclosing simulation combining hardware and software interaction.

Reference to Rompaey et al., U.S. Patent 5,870,588 issued February 9, 1999, is cited as disclosing a design method for hardware/software co-design.

Reference to Matsuoka et al., U.S. Patent 5,960,182 issued September 28, 1999, is cited as disclosing a hardware/software co-simulation method.

Reference to Tzori, U.S. Patent 6,202,044 issued March 13, 2001, and filed June 12, 1998, is cited as disclosing concurrent hardware/software co-simulation.

Reference to Klein et al., U.S. Patent 6,212,489 issued April 3, 2001, and filed June 8, 1998, is cited as disclosing an optimizing hardware/software co-verification system.

Reference to Becker et al., "An Engineering Environment for Hardware/Software Co-Simulation", Proceedings of the 29th ACM/IEEE Conference on Design Automation Conference, 1992, pages 129-134, is cited as creating a co-simulation engineering environment.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
February 15, 2003

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
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